M02140

Low Power 3.3 Volt Limiting Amplifier For Applications to 12.5 Gbps Low Power 3.3 Volt Limiting Amplifier

The M02140 is an integrated high-gain limiting amplifier intended for high-speed fiber optic based communications. Placed following the photodetector and transimpedance amplifier, the limiting amplifier provides the necessary gain to ensure full CML output swing even at its minimum input sensitivity.

Capable of operating over a very wide frequency range, the M02140 supports data and telecom applications up to 12.5 Gbps.

The M02140 includes an analog RSSI output and a programmable signal level detector allowing the user to set the threshold at which the loss of signal logic output is enabled.

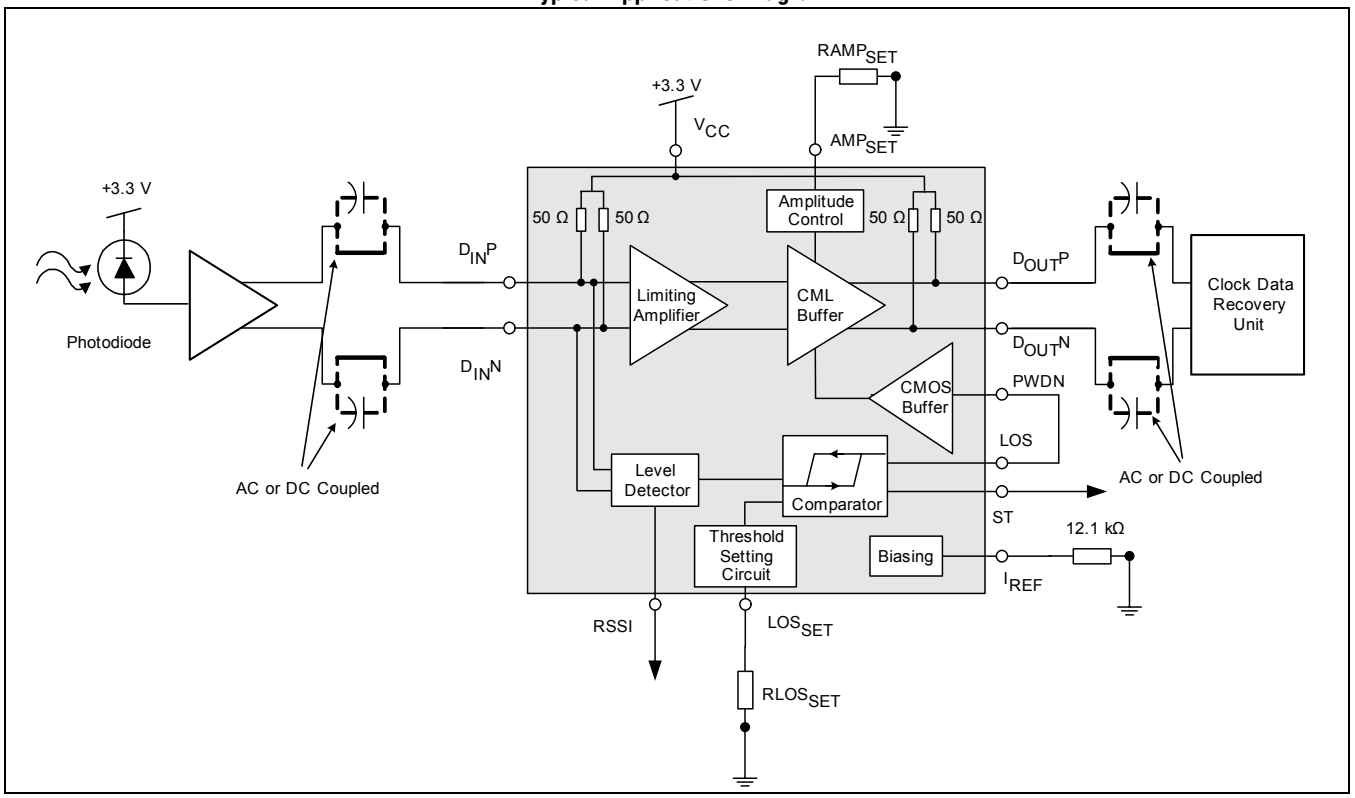
Applications

- STM-64/OC-192 SDH/SONET
- SDH/SONET with single or double FEC
- 10G Ethernet
- 10G Fiber Channel

Features

- M02140 wide dynamic range with typical 5.5 mV input sensitivity at 10.3 Gbps
- Received Signal Strength Indicator (RSSI)
- Programmable input signal level detect
- Fully differential
- CML data outputs with typical 23 ps rise and fall time
- Wide -40 to +85 °C operating temperature range
- Operates with +3.3 V supply
- Supply current typically 54 mA
- Programmable output amplitude (default 400 mVpp differential)
- On-chip DC offset cancellation circuit, no external capacitors needed

Typical Applications Diagram



Ordering Information

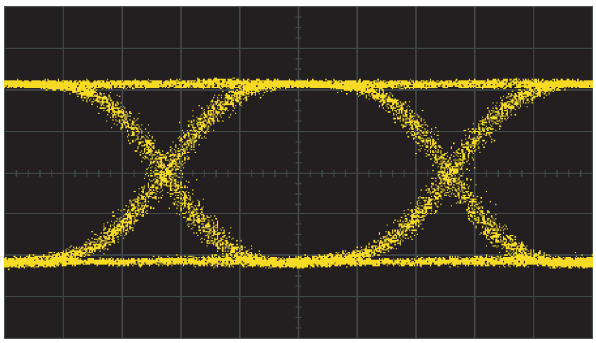
Part Number	Package	Operating Temperature
M02140-xx	24 pin MLF package	–40 °C to 85 °C

Note: xx represents the revision number. Please contact your local sales office for correct digits.

Revision History

Revision	Level	Date	ASIC Revision	Description
E	Preliminary	September 2004		Revised document layout.
D	Preliminary	June 2004		Update LOS specifications.
C	Preliminary	January 2004		Reformatted for new template.
B	Preliminary			
A	Preliminary			Initial Release.

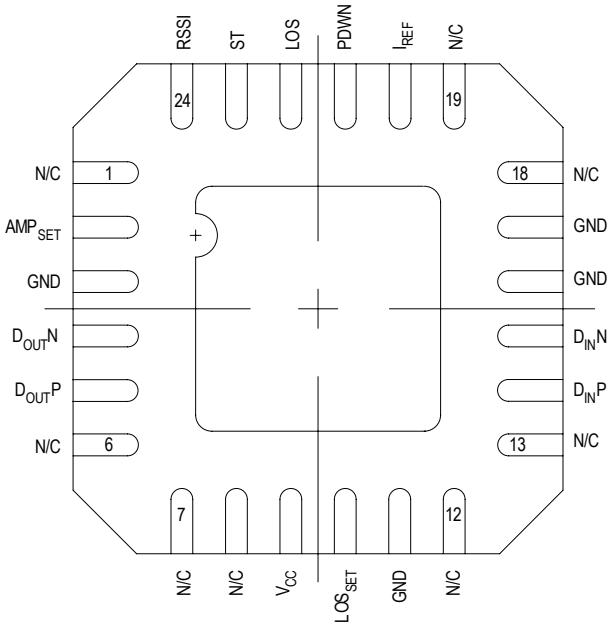
Typical Eye Diagram



Conditions 10 mVpp differential input
10.3 Gbps, Pattern 2^{23}-1
LOW output CML level

Scale Time 20 ps/Div.
Amp 50 mV/Div

Pin Configuration



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage (V_{CC} - GND)	-0.4 to +4.0	V
T_A	Operating ambient temperature	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C
$D_{OUT}P$, $D_{OUT}N$	Output pins voltage	V_{CC} - 0.4 to V_{CC} + 0.4	V
$D_{IN}P$, $D_{IN}N$	Data input pins voltage	V_{CC} - 0.32 to V_{CC} + 0.32	V
AMP_{SET}	Output amplitude setting pin voltage	GND to +0.1	V
LOS_{SET}	Signal detect threshold setting pin voltage	GND to +3.6	V
PWDN	Output enable pin voltage	GND to +3.6	V
I_{REF}	Current into Reference input	+ 0 to -120	µA
RSSI	RSSI pin voltage	+1 to +3.6	V
I(ST)	Current into Status pin	+1500 to -100	µA
I(LOS)	Current into Loss Of Signal pin	+1500 to -100	µA

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply (V_{CC} - GND)	3.3 ± 5%	V
Operating ambient temperature	-40 to +85	°C

Note: The package bottom must be adequately grounded to ensure correct thermal and electrical performance. It is recommended that a minimum of four vias be used with 0.3 to 0.33 mm diameter and 1.0 to 1.2 mm pitch to contact a ground plane.

1.3 DC Characteristics

(V_{CC} = +3.3V ± 5%, T_A = -40°C to +85°C, Outputs connected to a 50 Ω load to V_{CC}, unless otherwise noted).

Typical values are at V_{CC} = 3.3 V and T_A = 25 °C, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{CC}	Supply current (I_{CC})	400 mVpp differential output amplitude	–	54	70	mA
		800 mVpp differential output amplitude	–	61	75	mA
$DataOut_L$	Single-ended CML output low	400 mVpp differential output amplitude, settled value, (R_{AMPSET} = 0 Ω, $D_{IN} \geq$ 20 mVpp)	V_{CC} - 0.22	V_{CC} - 0.2	V_{CC} - 0.18	V
		800 mVpp differential output amplitude, settled value, (R_{AMPSET} = 887 Ω, $D_{IN} \geq$ 20 mVpp)	V_{CC} - 0.44	V_{CC} - 0.4	V_{CC} - 0.36	V
$DataOut_H$	Single-ended CML output high	400 mVpp differential output amplitude, settled value, (R_{AMPSET} = 0 Ω, $D_{IN} \geq$ 20 mVpp)	V_{CC} - 0.02	–	V_{CC}	V
		800 mVpp differential output amplitude, settled value, (R_{AMPSET} = 887 Ω, $D_{IN} \geq$ 20 mVpp)	V_{CC} - 0.04	–	V_{CC}	V
$V_{IN(CM)}$	Data input common mode voltage range	Input swing between $V_{IN(MIN)}$ and $V_{IN(MAX)}$ (see Table 1.4)	V_{CC} - 0.250	–	V_{CC}	V
$R_{IN(DIFF)}$	Data input differential resistance		85	100	115	Ω
$Z_{OUT(DIFF)}$	Data output differential impedance		85	100	115	Ω
V_{OH}	ST/LOS output HIGH voltage	4.7 kΩ to V_{CC}	2.4	–	–	V
V_{OL}	ST/LOS output LOW voltage	4.7 kΩ to V_{CC}		–	0.4	V
V_{IH}	PWDN input HIGH voltage		2.0	–	V_{CC}	V
V_{IL}	PWDN input LOW voltage		0	–	0.8	V

1.4 AC Characteristics

(V_{CC} = +3.3V ± 5%, T_A = -40°C to +85°C, input bit rate = 10.3 Gbps, 2^{31} - 1 PRBS, unless otherwise noted).

Typical values are at V_{CC} = 3.3 V and T_A = 25 °C, unless otherwise noted.

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IN(MIN)}$	Input Sensitivity (1, 2, 3)	BER <10^{-10}, differential input	–	5.5	7	mV_{PP}
		BER <10^{-10}, single-ended input	–	–	7	mV_{PP}
		BER <10^{-12}, differential input	–	6.5	8	mV_{PP}
		BER <10^{-12}, 12.5 Gbps, differential input	–	9	–	mV_{PP}
$V_{IN(MAX)}$	Input Overload (1, 2)	BER <10^{-10}, differential input	1000	–	–	mV_{PP}
		BER <10^{-10}, single-ended input	500	–	–	mV_{PP}
E_N	Input referred noise	Measured differentially	–	450		μV_{RMS}
RJ	Random Jitter	20 mV_{PP} differential input, alternating 1-0 pattern	–	0.8	1.2	ps_{RMS}
		12.5 Gbps, 20 mV_{PP} differential input, alternating 1-0 pattern	–	0.8	1.2	ps_{RMS}
DJ	Deterministic Jitter (includes DCD)	20 mV_{PP} differential input	–	3.3	10	ps_{PP}
		20 mV_{PP} differential input, 12.5 Gbps	–	3.7	12	ps_{PP}
DCD	Duty Cycle Distortion	Alternating 1-0 pattern at 2488 Mbps(4)	–	1.3	5	ps
tr, tf	Data outputs rise and fall time (input > 20 mV_{PP} differential)	400 mVpp differential output amplitude, (R_{AMPSET} = 0 Ω) (5)	–	23	30	ps
		800 mVpp differential output amplitude, (R_{AMPSET} = 887 Ω) (5)	–	28	40	ps
f_L	Small signal -3 dB low frequency cut off	Excluding AC coupling capacitors	–	50	75	kHz
LOS_{TH}	LOS programmable threshold range	Differential input	10	–	100	mV_{PP}
V_{HYST}	LOS hysteresis	Electrical LOS threshold across programmable threshold range	2	4.5 (6)	7.5	dB
$ASSERT_{LOW}$	Low Input R_{LOS} LOS Assert threshold	R_{LOS} = 4.99 kΩ, differential input	8	12.5	–	mV_{PP}
$DEASSERT_{LOW}$	Low Input R_{LOS} LOS De-Assert threshold	R_{LOS} = 4.99 kΩ, differential input	–	21	32	mV_{PP}

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$ASSERT_{MED}$	Medium Input R_{LOS} LOS Assert threshold	R_{LOS} = 4.75 kΩ, differential input	16	25	–	mV_{PP}
$DEASSERT_{MED}$	Medium Input R_{LOS} LOS De-Assert threshold	R_{LOS} = 4.75 kΩ, differential input	–	41	65	mV_{PP}
$ASSERT_{HI}$	High Input R_{LOS} LOS Assert threshold	R_{LOS} = 4.02 kΩ, differential input	48	75	–	mV_{PP}
$DEASSERT_{HI}$	High Input R_{LOS} LOS De-Assert threshold	R_{LOS} = 4.02 kΩ, differential input	–	125	190	mV_{PP}
T_{LOS_ON}	Time from LOS state until LOS is asserted (ST de-asserted)	LOS assert time after 1 Vpp input signal or smaller is turned off; LOS assert level set to 10 mV	–	13.5 (7)	80	µs
T_{LOS_OFF}	Time from non-LOS state until LOS is de-asserted (ST asserted)	LOS de-assert time after input crosses LOS de-assert level; LOS de-assert level set to 20 mV with applied input signal of 30 mVpp or greater	–	7 (8)	80	µs

Notes:

1. 5.5 - 1000 mVpp differential input translates to 2.75 - 500 mVpp for each single-ended input. See Figure 1-1.

2. When driven with a single-ended input, the unused input is DC-coupled through 50 Ω to the common mode level of the driven input. See Figure 1-1.

3. There is no difference in performance using a 2^{23} - 1 PRBS versus a 2^{31} - 1 PRBS.

4. Measured as [(pulse width of a one) - (pulse width of a zero)]/2. Pulse width measured at 50% points.

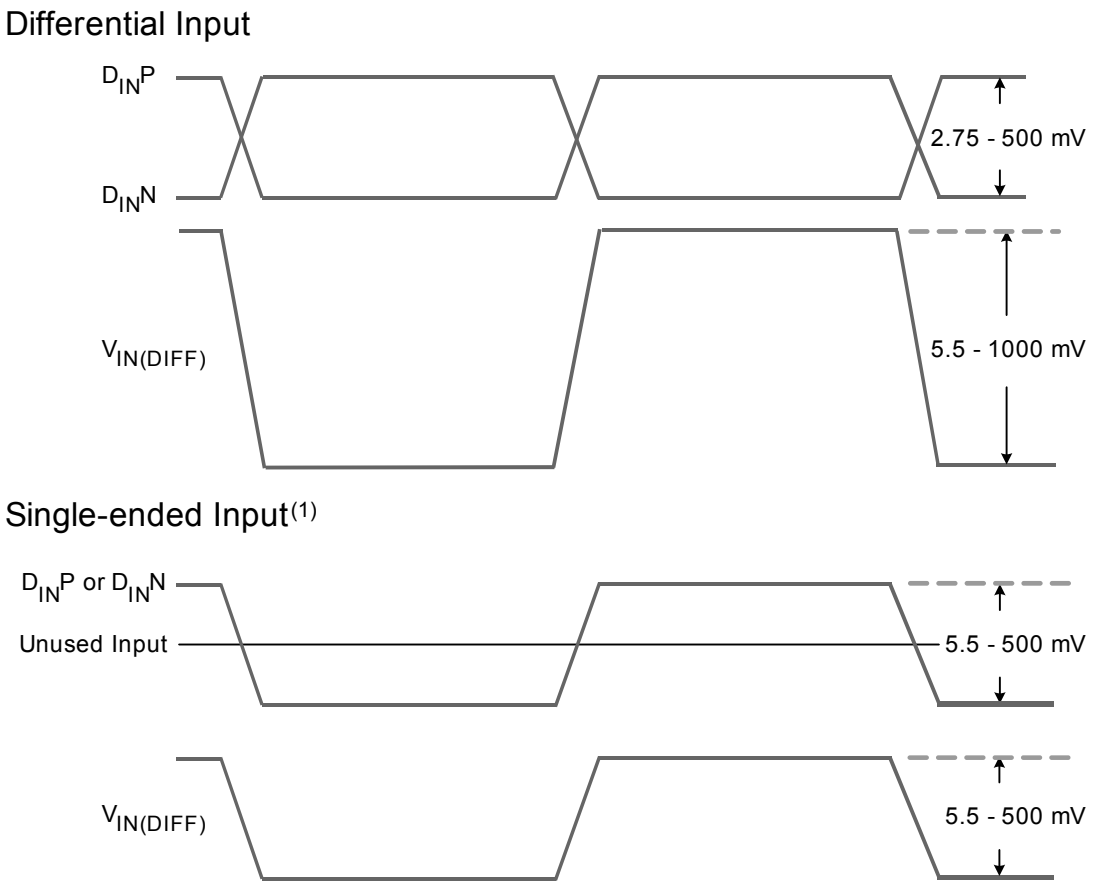
5. The rise and fall times are using the 20% to 80% thresholds at each output. The output is DC-coupled into 50 Ω to V_{CC}.

6. This corresponds to 2.25 dB optical.

7. With V_{IN_DIFF} = 1 Vpp, typical times decrease as V_{IN_DIFF} decreases.

8. With V_{IN_DIFF} = 30 mVpp, typical times decrease as V_{IN_DIFF} increases.

Figure 1-1. Data Input Requirements



Note:

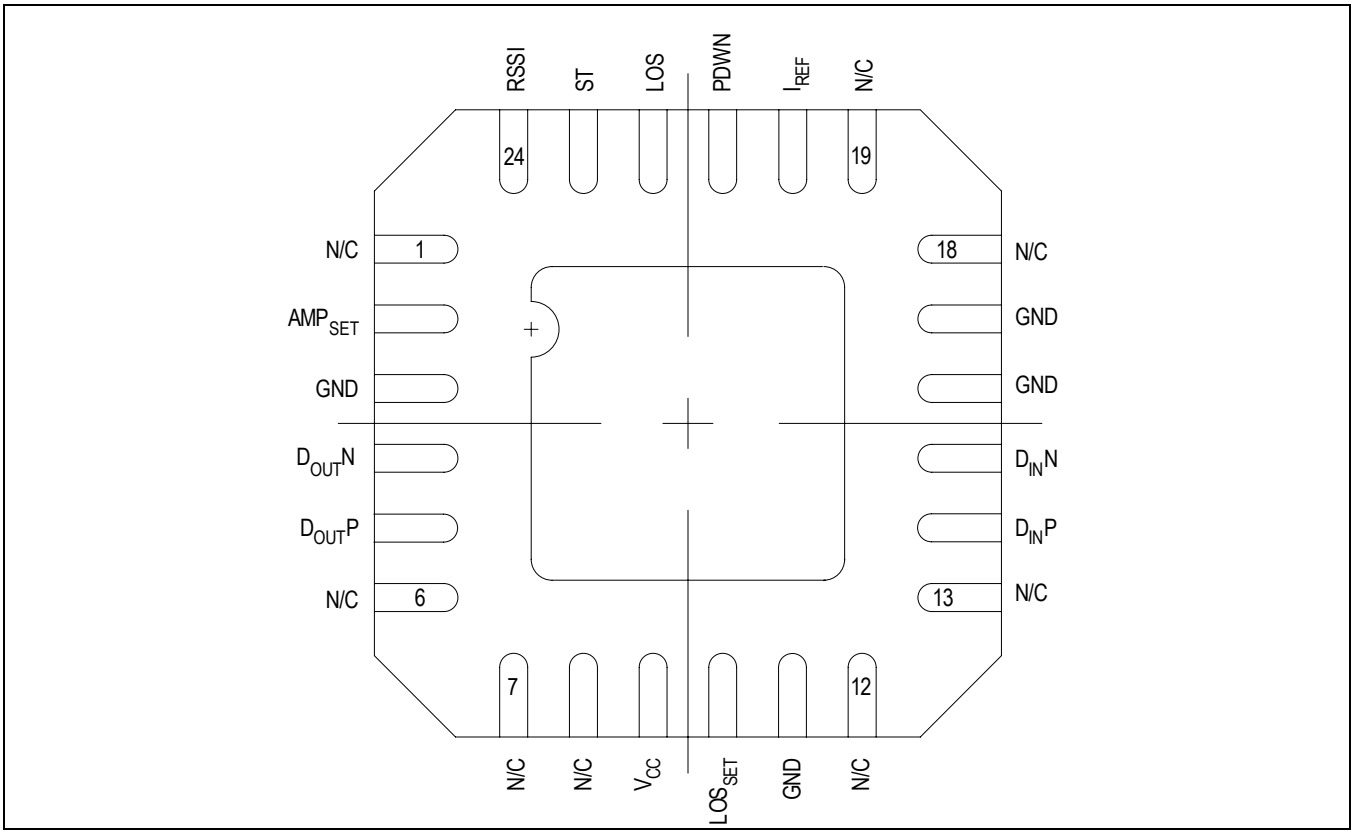
1. Unused input AC-coupled through 50 Ω to V_{CC} when used input is AC-coupled to TIA; Unused input DC-coupled through 50 Ω to the common mode level of TIA output when the used input is DC-coupled to the TIA

2.0 Pin Definitions

Table 2-1. Pin Descriptions

MLF Pin Number	Name	Function
1	N/C	Not connected. (Not internally bonded, can be connected to any DC potential including ground)
2	AMP_{SET}	Enables setting of output voltage swing from 400 mVpp differential to 800 mVpp differential using an external 1% resistor (R_{AMPSET}) to ground
3	GND	Ground
4	$D_{OUT}N$	Inverting differential data output. CML output internally terminated 50 Ω to V_{CC}
5	$D_{OUT}P$	Non-inverting differential data output. CML output internally terminated 50 Ω to V_{CC}
6, 7, 8	N/C	Not connected. (Not internally bonded, can be connected to any DC potential including ground)
9	V_{CC}	Positive supply
10	LOS_{SET}	Loss of signal threshold setting input. User programmed with 1% resistor (R_{LOS}) to V_{CC}
11	GND	Ground
12, 13	N/C	Not connected. (Not internally bonded, can be connected to any DC potential including ground)
14	$D_{IN}P$	Non-inverting data input. Internally terminated 50 Ω to V_{CC}
15	$D_{IN}N$	Inverting data input. Internally terminated 50 Ω to V_{CC}
16, 17	GND	Ground
18, 19	N/C	Not connected. (Not internally bonded, can be connected to any DC potential including ground)
20	I_{REF}	Reference current termination. Must be connected to ground through an external 12.1 kΩ, 1% resistor (R_{REF}). This connection generates an on-chip reference current
21	PWDN	CMOS compatible logic input. When high, the output stage current is switched off, this will make $D_{OUT}P$ and $D_{OUT}N$ both equal to V_{CC}. Data outputs are enabled when PWDN is low or floating
22	LOS	Loss of Signal Indicator. Asserted when input signal levels falls below threshold established at LOS_{SET}. May be externally connected to the PWDN pin to enable the automatic jam function
23	ST	Input signal level status. Logical inverse of LOS. This output is LOW when the input signal is below the threshold set at LOS_{SET}. This is an open drain output with an internal 100 kΩ pull-up
24	RSSI	Received signal strength indicator. The output amplitude is proportional to the received input signal level
EP	Exposed Paddle	Package backside. Must be conductively connected to ground

Figure 2-1. 24 Pin (4 x 4mm) MLF top view



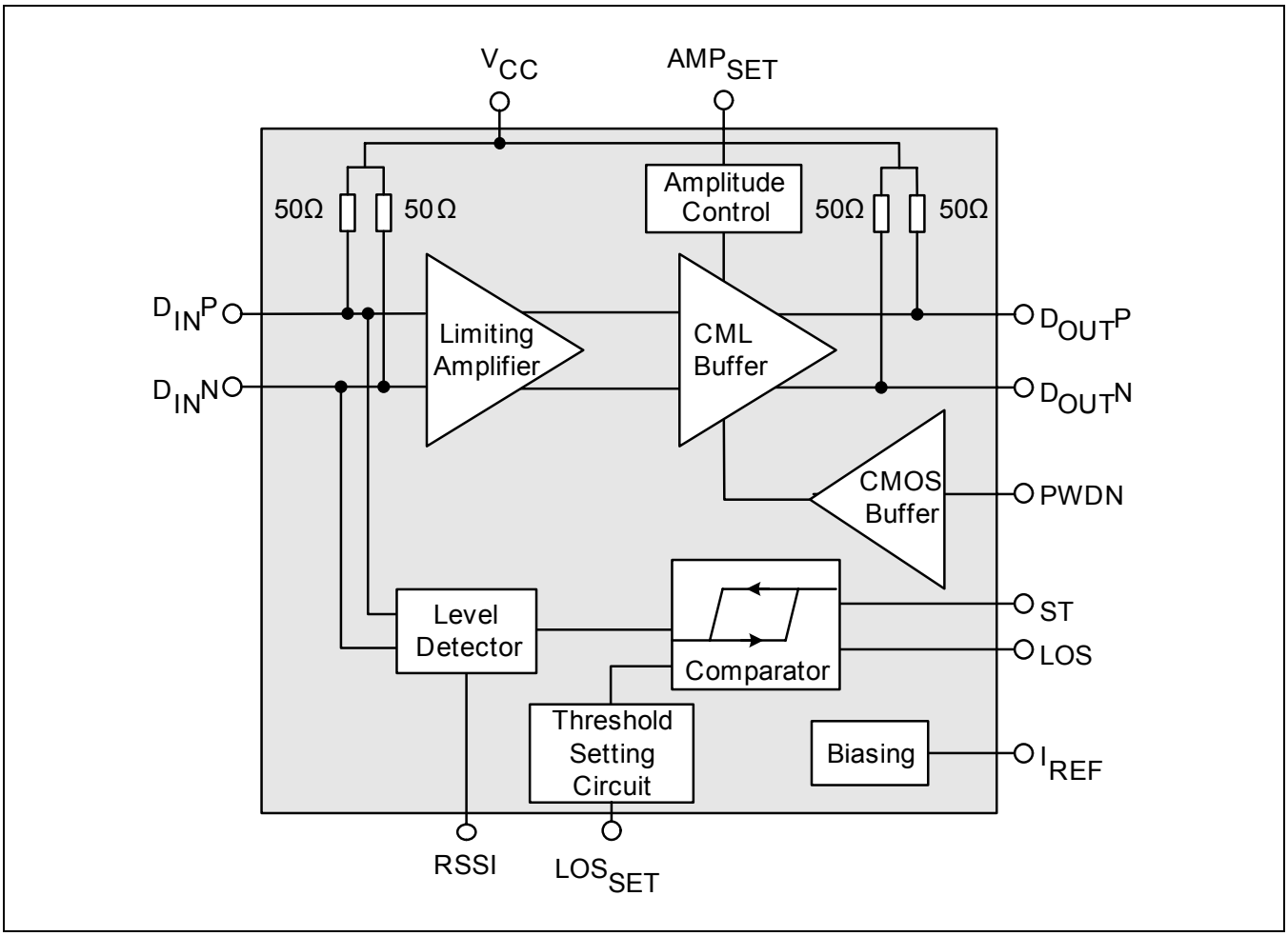
3.0 Functional Description

3.1 Overview

The M02140 is a high-gain limiting amplifier for applications up to 12.5 Gbps, and incorporates a limiting amplifier, a CML buffer and an input signal level detection circuit. The M02140 also features a fully integrated DC-offset cancellation loop that does not require any external components.

The user is provided with the flexibility to set the output amplitude levels and the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the PWDN input.

Figure 3-1. M02140 Block Diagram



3.2 General Description

3.2.1 Inputs

The data inputs are internally biased to V_{CC} via 50 Ω resistors, and may be AC or DC-coupled. Note that if the inputs are AC-coupled, the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance (It is recommended a capacitor of 2 to 10 nF be used). The coupling capacitor should also be of sufficient quality as to pass the high frequency content of the input data stream.

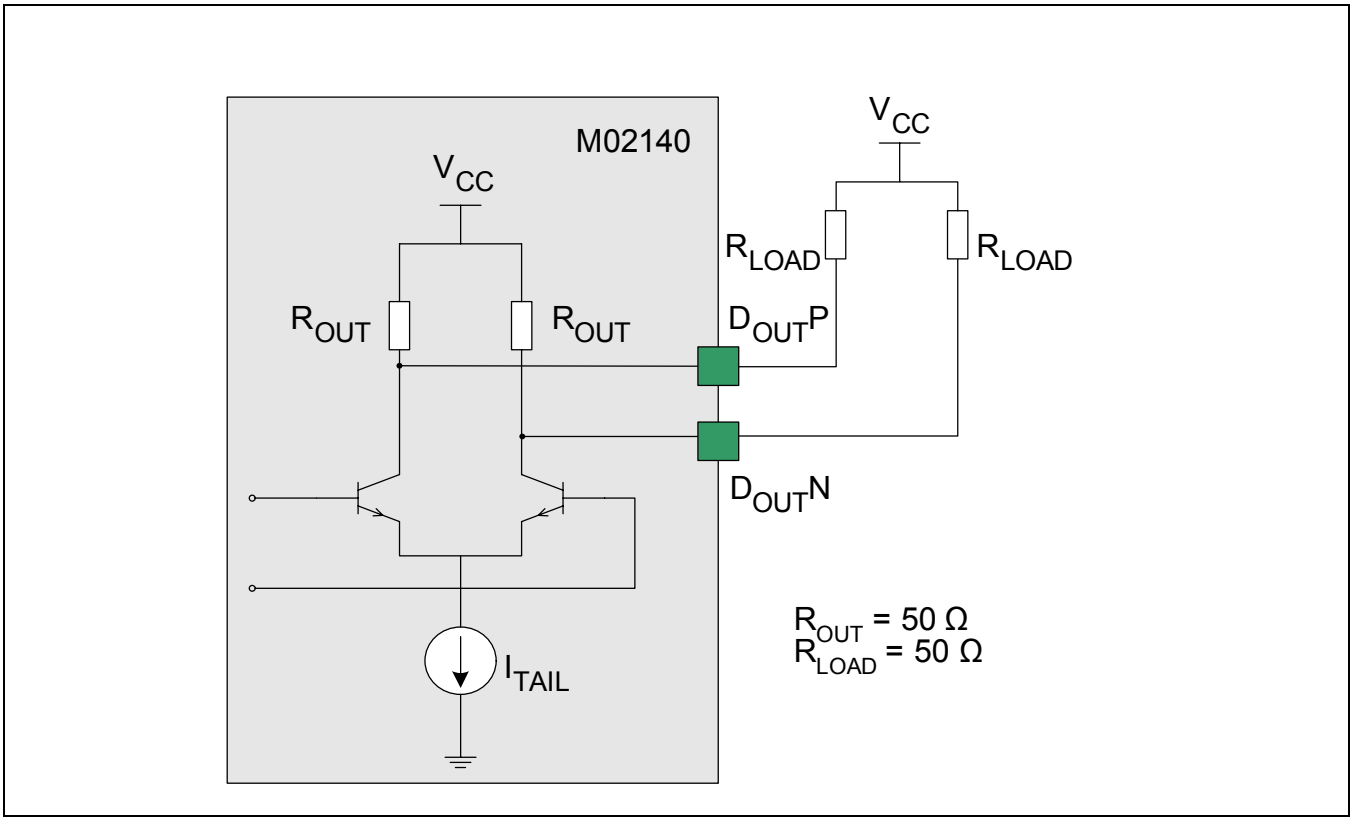
3.2.2 DC Offset Compensation

The M02140 contains internal DC feedback requiring no external components to remove the effects of DC offsets and to act as a DC auto-zero circuit. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off typically is less than 50 kHz.

3.2.3 Outputs

The basic output configuration is as shown in Figure 3-2. The external resistor R_{AMPSET} controls the value of I_{TAIL}. The output swing is linearly proportional to the value of R_{AMPSET}. It is possible to set the output voltage swing linearly between 400 mVpp differential and 800 mVpp differential, when the outputs are properly terminated. See the applications information section for further details on setting the output swing amplitude.

Figure 3-2. Data Outputs



3.2.4 Received Signal Strength Indicator (RSSI)

The RSSI output voltage is proportional to the log of the input signal amplitude as shown in Figure 3-3 (the RSSI output voltage is linearly proportional to the Optical Modulation Amplitude (OMA)). An external 4.7 nF capacitor must be connected from the RSSI output to V_{CC} as shown in Figure 3-4. The capacitor integrates the RSSI output and also sets the loss of signal reaction time. The RSSI voltage is compared with a selectable reference to determine loss of signal as described in the next section.

Figure 3-3. RSSI Output

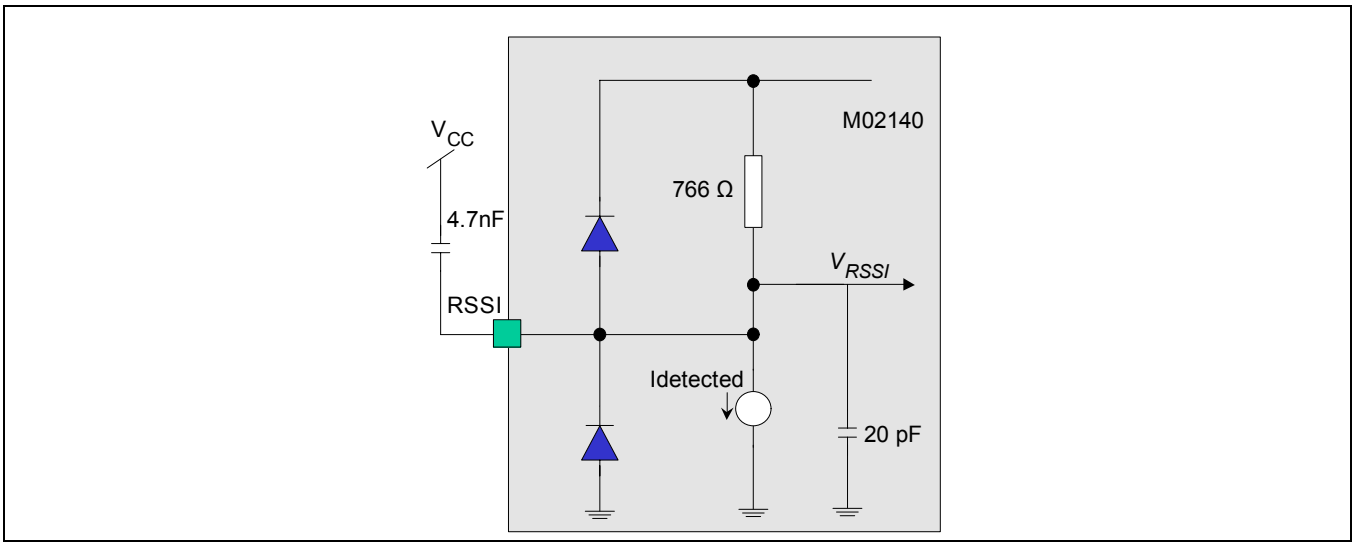
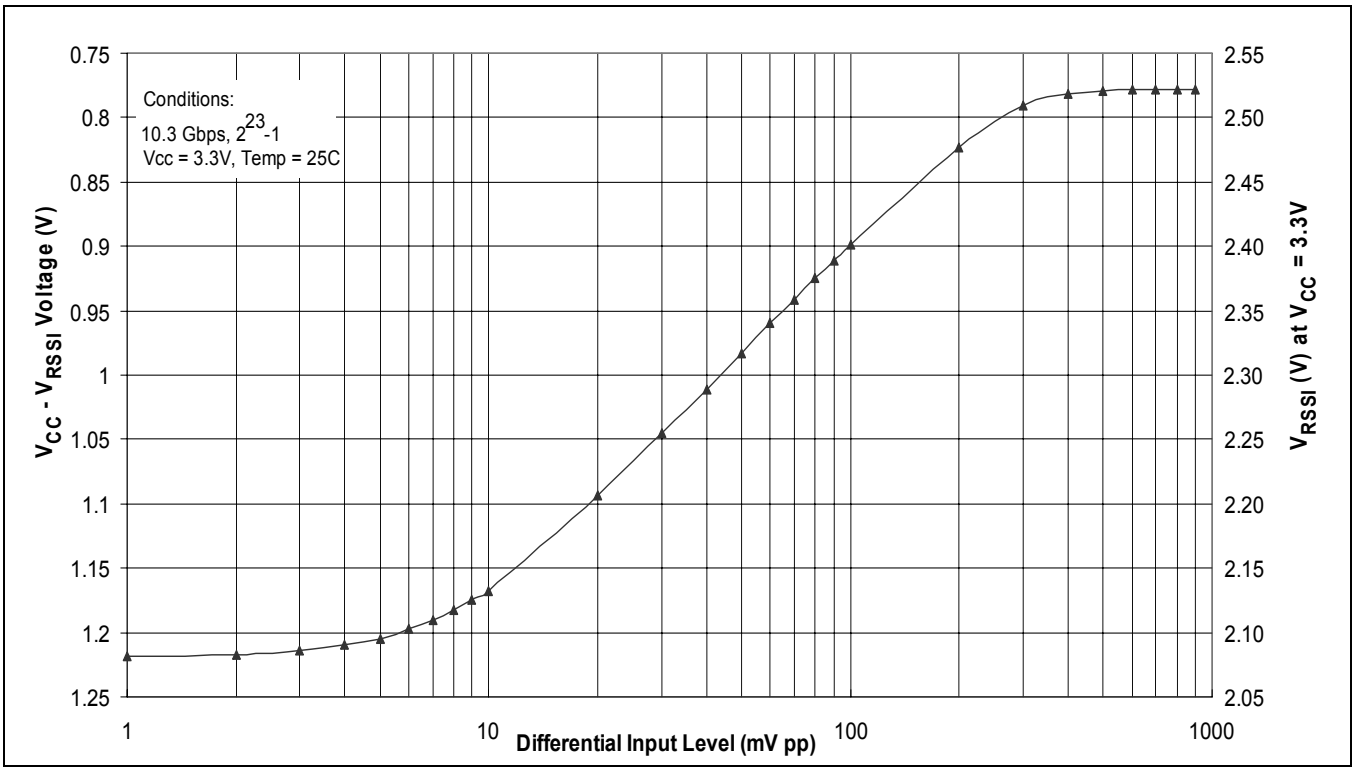


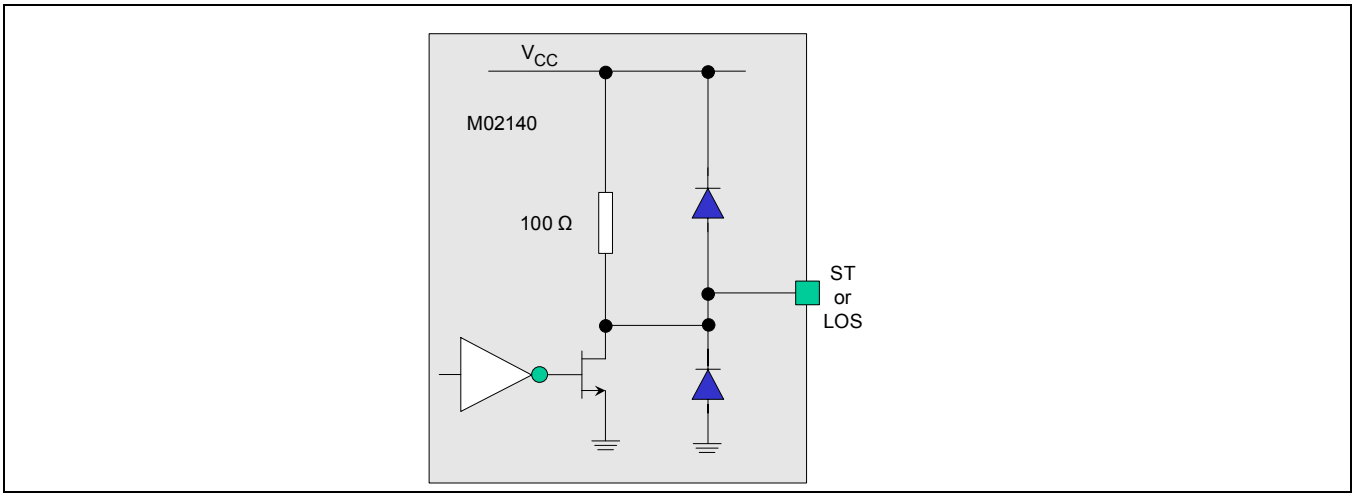
Figure 3-4. RSSI Transfer Function



3.2.5 Loss of Signal (LOS)

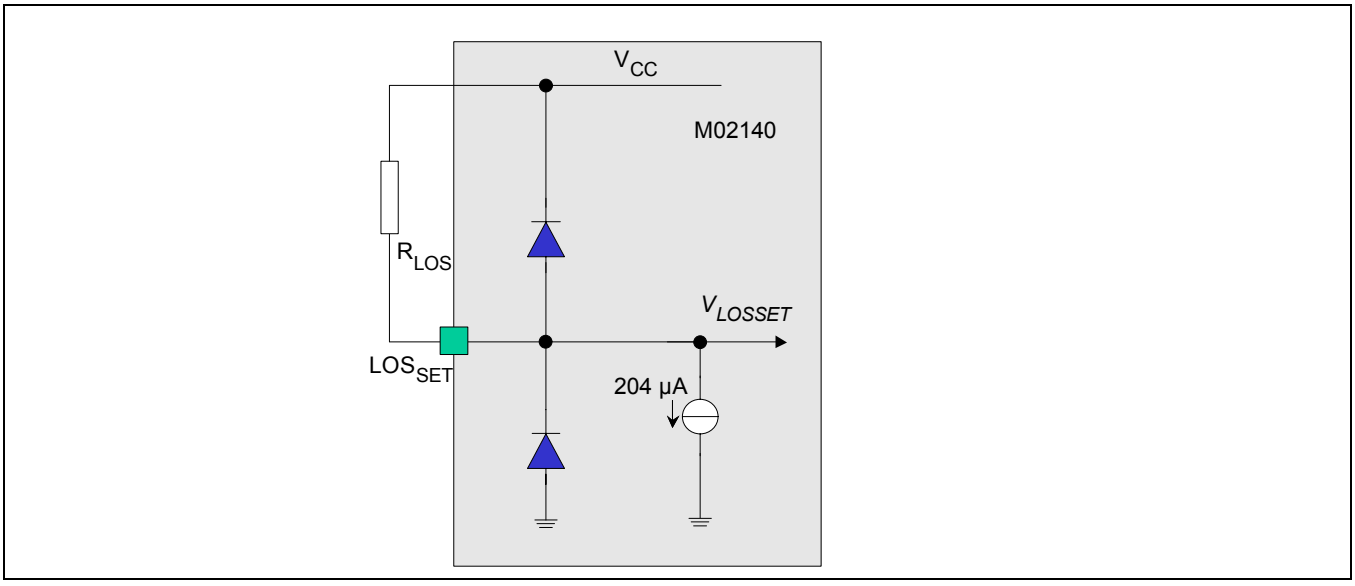
The M02140 features input signal level detection over an extended range. Using an external resistor, R_{LOS}, between pin LOS_{SET} and V_{CC}, the user can program the input signal threshold. The signal detect status is indicated on the LOS and ST open-drain output pins shown in Figure 3-5. These two pins are inverses of each other: the LOS signal is active when the signal is below the threshold value, ST is active when the signal is above the threshold value. The signal detection circuitry has the equivalent of 4.5dB (typical) electrical hysteresis.

Figure 3-5. LOS and ST Outputs



R_{LOS} establishes a threshold voltage at the LOS_{SET} pin as shown in Figure 3-6. The input signal develops a voltage at the RSSI pin as shown in Figure 3-4. As described in the RSSI section, this voltage is proportional to the input signal peak to peak value. The voltage at LOS_{SET} is internally compared to the voltage at the RSSI ($V_{(RSSI)}$) pin. When the voltage at $V_{(RSSI)}$ is less than $V_{(LOSSET)}$, LOS is asserted (ST de-asserted) and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis, LOS is de-asserted (ST asserted). See the applications section for the selection or R_{LOS}.

Figure 3-6. LOSset Input



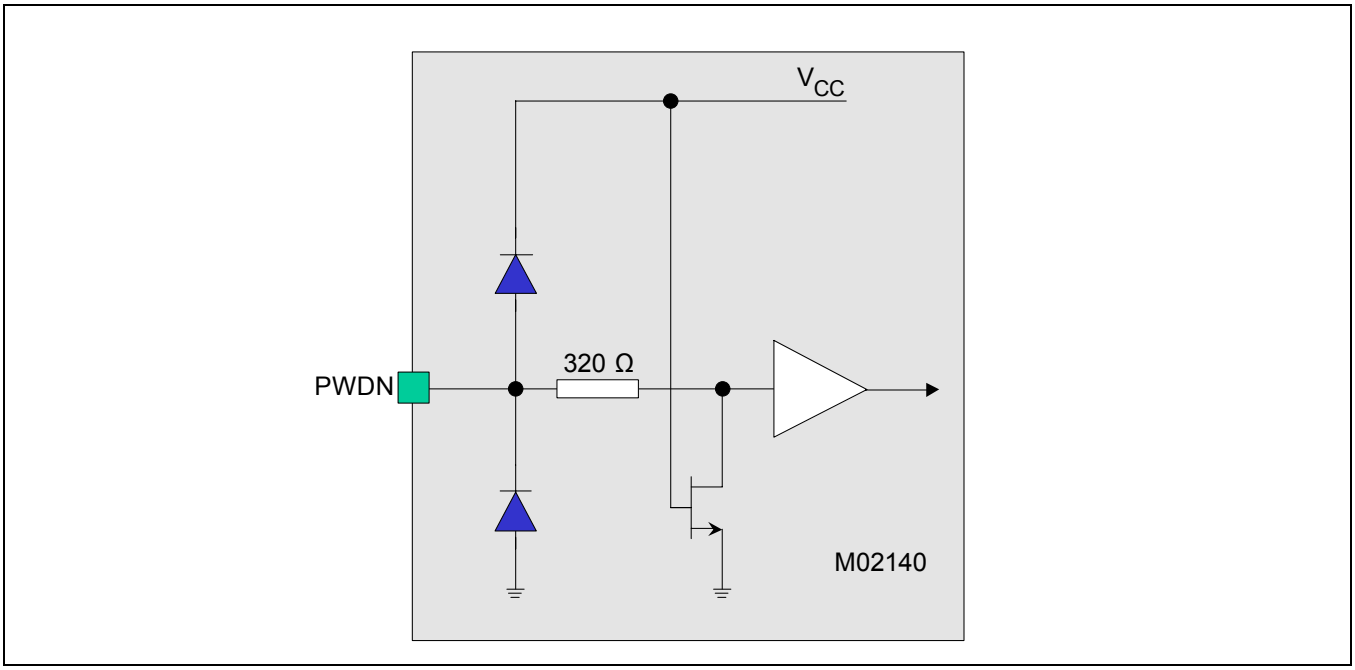
3.2.6 Squelch Function (Jam) using PWDN

When asserted, the active high power down (PWDN) pin forces the outputs to a high state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present (“squelch”).

In order to implement this function, LOS should be connected to the PWDN pin shown in Figure 3-7, thus forcing the data outputs to V_{CC} when the signal falls below the threshold.

Note that LOS_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

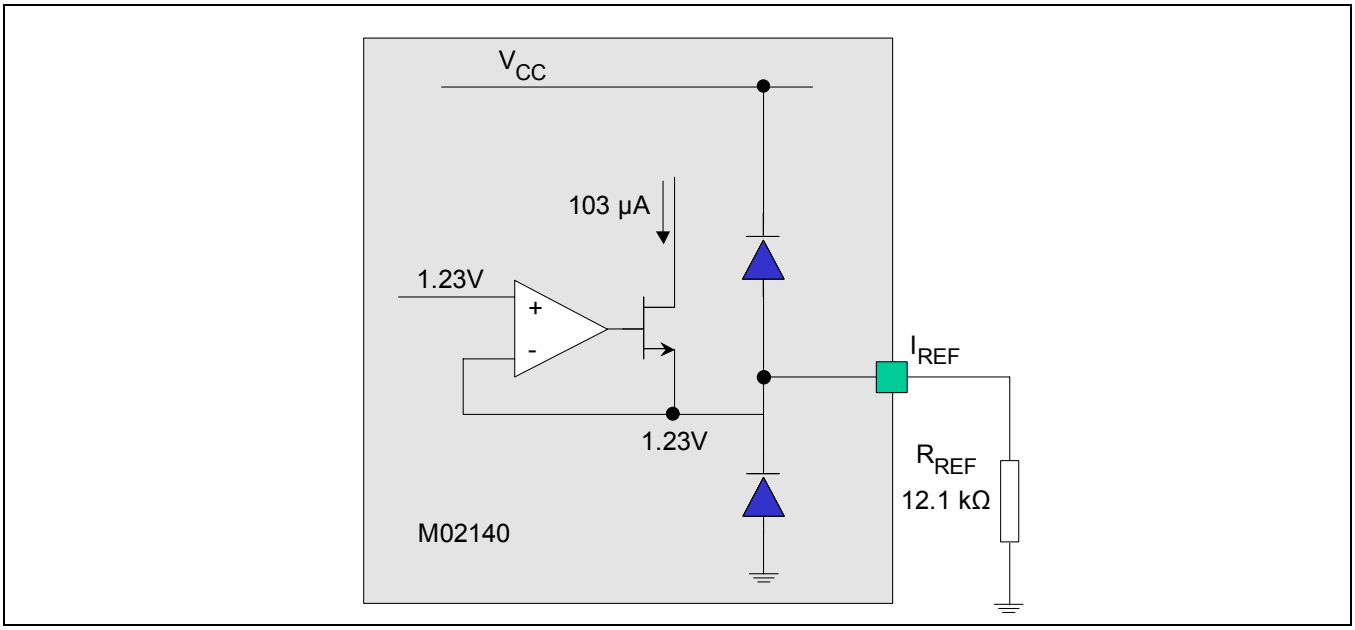
Figure 3-7. Power Down (PWDN)



3.2.7 Bias Generation

The M02140 contains an accurate on-chip bias circuit requiring an external 12.1 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to define an on-chip reference current.

Figure 3-8. Reference Current Connection



4.0 Applications Information

4.1 Setting the Output Swing Level

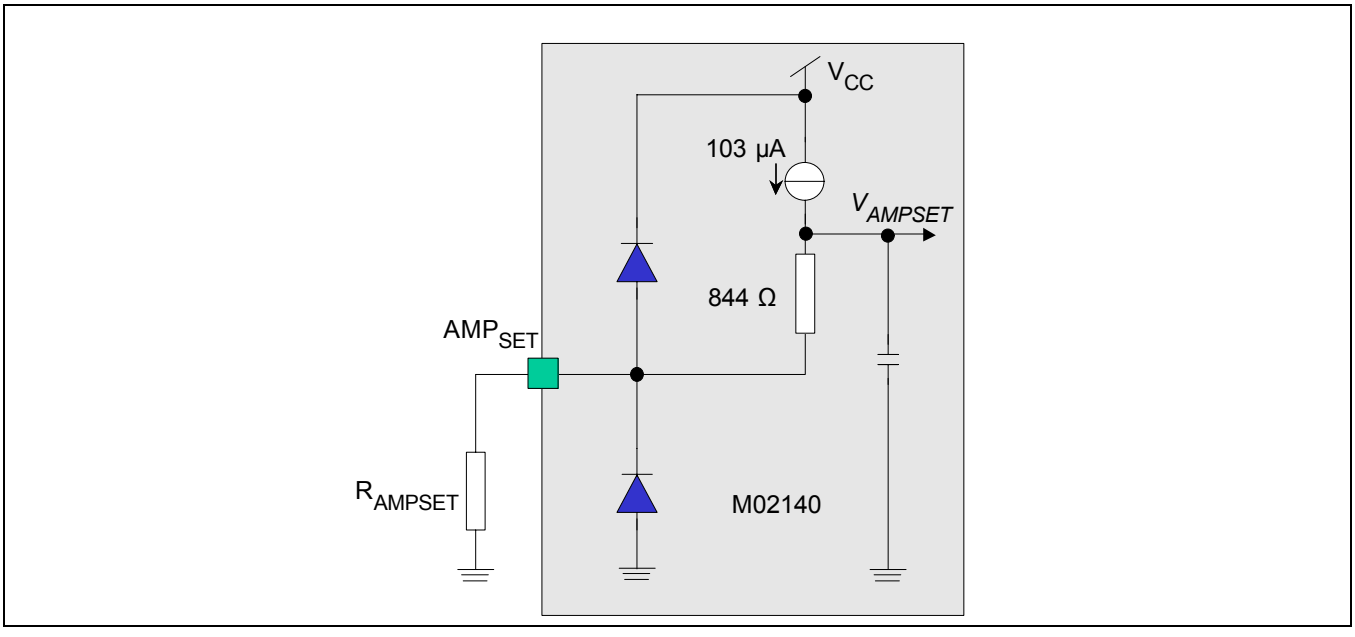
The output circuit is shown in Figure 3-2. It is basically a differential pair with a tail current of I_{TAIL}. The load of the differential pair is formed by the parallel combination of R_{OUT} and R_{LOAD} for high frequencies where the output AC-coupling capacitor can be considered as a short circuit (50 || 50 = 25 Ω). The single-ended output voltage swing is given by EQ.1:

$$V_{PP\text{-}SE} = I_{TAIL} \times (R_{OUT} \parallel R_{LOAD}) \qquad \text{EQ. 1}$$

The required minimum voltage swing sets I_{TAIL} and I_{TAIL} determines the output power consumption. The minimum voltage swing depends on the application. Therefore, M02140 provides the user the flexibility to optimize the voltage swing and the output power consumption in his own application by setting I_{TAIL} using an external resistor (R_{AMPSET}) shown in Figure 4-1. To select the required swing, use the following equation (EQ.2):

$$I_{TAIL} = 8\ mA + (R_{AMPSET} \times 9.0 \times 10^{-3})\ mA \qquad \text{EQ. 2}$$

Figure 4-1. AMPset



The minimum I_{TAIL} is 8mA and occurs when the AMPSET pin is directly connected to ground. The resulting voltage swing is 200 mVpp, single-ended (= 8 mA x 25 Ω). This is sufficient for most applications. If it is necessary, the voltage swing can be increased at the expense of the power consumption by connecting an external resistor R_{AMPSET} between the AMP_{SET} pin and ground. The value of R_{AMPSET} can be calculated from EQ.2. A resistor of 887 Ω results in 16 mA tail current which delivers a voltage swing of 400 mVpp, single-ended (16 mA x 25 Ω).

4.2 Setting the Signal Detect Level

Using Figure 4-2, the value for R_{LOS} is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Figure 4-2.

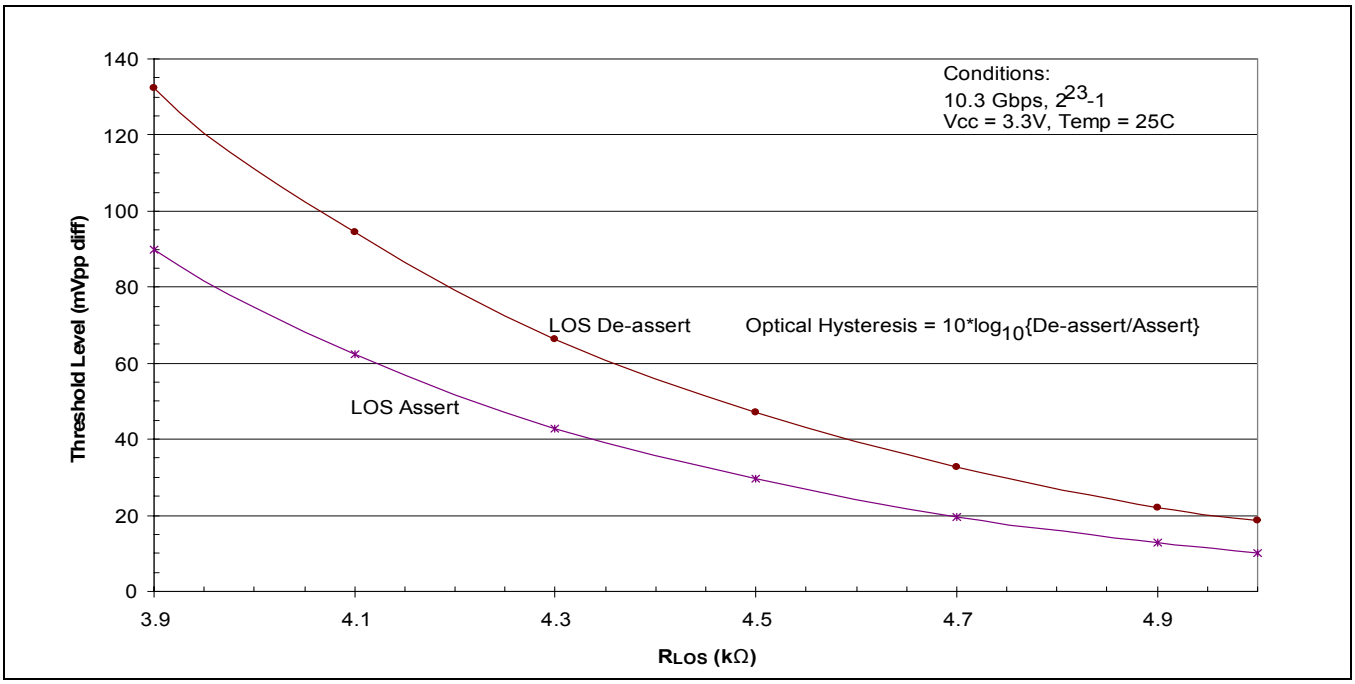
Three example R_{LOS} resistor values are given in Table 7.

From Figure 4-2, it is apparent that small variations in R_{LOS} cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the RSSI voltage and the input signal level. It is recommended that a 1% resistor be used for R_{LOS} and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02140.

Table 4-1. RLOS Resistor Values

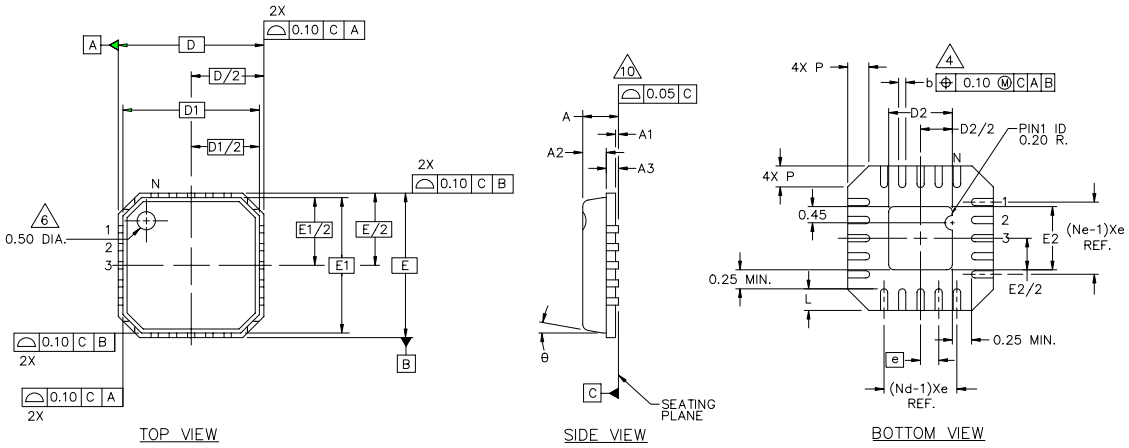
LOS Assert Threshold VIN (mV pp) differential	R_{LOS} (kΩ) (nearest 1% value)
10	4.99
20	4.64
50	4.22
75	4.02

Figure 4-2. Loss of Signal Characteristic

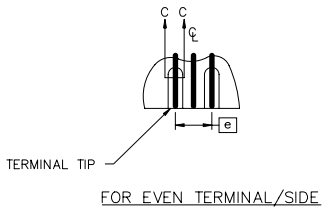


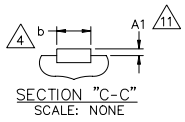
5.0 Package Specification

Figure 5-1. Package Information



Note: View is for a 20 pin package. All dimensions in the tables apply for the 24 pin package





SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	2.19	2.34	2.49	
E2	2.19	2.34	2.49	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

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